AMENDMENT AND RESPONSE UNDER 37 CFR § 1.116
Serial Number: 10/716,755
Filing Date: November 19, 2003
Title: FLOATING-BODY DRAM WITH TWO-PHASE WRITE
Assignee: Intel Corporation

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IN THE CLAIMS

Please amend the claims as follows:

Claims 1-6. (Canceled)

7. (Previously Presented) A method comprising writing data to floating-body memory cells in two phases, wherein each of the two phases utilizes a different word line voltage on a selected word line, and at least one of the two phases utilizes a different word line voltage on an unselected word line.

8. (Previously Presented) The method of claim 7 wherein a first phase writes to a first subset of memory cells coupled to the selected word line.

9. (Original) The method of claim 8 wherein the first phase discharges floating bodies of the first subset of memory cells.

10. (Original) The method of claim 8 wherein the first phase comprises reducing a voltage on at least one bit line to turn on a diode formed at least partially by a floating body of a transistor.

11. (Previously Presented) The method of claim 8 wherein a second phase writes to a second subset of memory cells coupled to the selected word line.

12. (Original) The method of claim 11 wherein the second phase charges floating bodies of the second subset of memory cells.

13.   (Original) The method of claim 11 wherein:

the first phase includes providing a first drain voltage on the first subset of memory cells and a second drain voltage on cells other than the first subset; and

the second phase includes providing a third drain voltage on the second subset of memory cells and a fourth drain voltage on cells other than the second subset.

14.   (Previously Presented) A method comprising:

providing a first voltage on a selected word line coupled to a plurality of memory cells;

writing "0" to at least one of the plurality of memory cells;

providing a second voltage on the selected word line;

increasing a voltage on unselected word lines; and

writing "1" to at least one of the plurality of memory cells.

15.   (Original) The method of claim 14 wherein each of the plurality of memory cells includes a single transistor.

16.   (Previously Presented) The method of claim 15 wherein the selected word line is coupled to gates of the single transistors.

17.   (Original) The method of claim 15 wherein the second voltage is higher than the first voltage.

18.   (Original) The method of claim 14 wherein each of the plurality of memory cells comprises a floating-body transistor.

19.   (Previously Presented) The method of claim 14 wherein writing a "0" comprises providing a voltage on a selected bit line to turn on a diode.

20.   (Previously Presented) The method of claim 14 wherein writing a "1" comprises providing a voltage on a selected bit line to generate an impact ionization current.

21.   (Currently Amended) An apparatus comprising:

        a plurality of rows of memory cells; and

        a plurality of word line drivers, wherein each of the plurality of word line drivers is coupled to one of the plurality of rows of memory cells, the word line drivers to generate a first voltage when holding the state of the memory cells, a second voltage on a selected word line when writing a "0," a third voltage on the selected word line when writing a "1," and a fourth voltage on unselected word lines when writing a "1[[.]]," wherein the fourth voltage is greater than the first voltage.

22.   (Previously Presented) The apparatus of claim 21 wherein the plurality of word line drivers are adapted to generate at least four different voltages.

23.   (Previously Presented) The apparatus of claim 22 wherein the plurality of word line drivers are adapted to generate at least five different voltages.

24.   (Previously Presented) The apparatus of claim 21 wherein the plurality of rows of memory cells comprise floating-body transistors.

25.   (Currently Amended) A memory device comprising:

        floating-body single transistor memory cells; and

a plurality of word line drivers coupled to the floating-body single transistor memory cells; ~~and~~ to increase a voltage on unselected word lines during a memory write cycle in which selected ones of the floating-body single transistor memory cells have their bodies charged.

~~a plurality of bit line drivers coupled to the floating-body single transistor memory cells;~~

~~wherein the memory device is adapted to perform two-phase writes in which the plurality of word line drivers drive a first voltage during a first phase to write one logical value, and the plurality of word line drivers drive a second voltage during a second phase to write a complementary logical value, and wherein the word line drivers are adapted to drive the first voltage during the first phase when coupled to a selected row, and to drive a third voltage during the first phase when coupled to an unselected row.~~

26.   (Canceled)

27.   (Canceled)

28.   (Currently Amended) An electronic system comprising:

an antenna;

a first integrated circuit coupled to the antenna; and

a second integrated circuit including a memory device, the memory device comprising floating-body single transistor memory cells; and a plurality of word line drivers coupled to the floating-body single transistor memory cells to increase a voltage on unselected word lines during a memory write cycle in which selected ones of the floating-body single transistor memory cells have their bodies charged. ~~; and a plurality of bit line drivers coupled to the floating-body single transistor memory cells; wherein the memory device is adapted to perform two-phase writes in which the plurality of word line drivers drive a first voltage during a first phase to write one logical value, and the plurality of word line drivers drive a second voltage during a second phase to write a complementary logical value, and wherein the word line drivers~~

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are adapted to drive the first voltage during the first phase when coupled to a selected row, and to

drive a third voltage during the first phase when coupled to an unselected row.

29.   (Canceled)

30-32. (Canceled)

33.   (Previously Presented) A method comprising increasing a voltage on unselected word
lines during a memory device write cycle in which selected floating body transistors have their
bodies charged.

34.   (Previously Presented) The method of claim 33 wherein increasing a voltage on
unselected word lines comprises increasing gate voltages on unselected transistors in selected
columns to reduce a gate-to-drain voltage on the unselected transistors.

35.   (Previously Presented) the method of claim 33 wherein an increased voltage on unselected
word lines is chosen to keep a gate-to-drain voltage on unselected transistors within process
imposed limits when a drain voltage is increased to charge a body of a selected transistor.